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EXAMINER

TRAN, THIEN F

ART UNIT PAPER NUMBER

2811

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Allowable Subject Matter

The indicated allowability of claims 53-55 and 60-63 is withdrawn in view of the newly discovered reference(s) to Davis et al. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 60-62 are rejected under 35 U.S.C. 102(e) as being anticipated by Davis et al. (US 2003/0155642).

Davis et al. discloses a method of designing an integrated circuit, the method comprising generating a representation of a shielding mesh (Figs. 4, 5; paragraph 0034) having a first layer and a second layer, the first layer including a first conductor (71, 38), the second layer including a second conductor (67, 37); and generating a representation of two vias 47, each of the two vias connecting from the first conductor to the second conductor.

Regarding claim 61, the first conductor 38 and the second conductor 37 are not parallel.

Regarding claim 62, the first conductor and the second conductor are in close proximity.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (US 2003/0155642).

Davis et al. does not specifically disclose the method being performed at least in part by an electronic design automation (EDA) tool. However, using EDA tool is a well-known method in the art to design integrated circuits. Therefore, designing the integrated circuit of Davis et al. using known EDA tool would have been obvious modification.

Claims 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crafts (US 5,288,949) in view of Davis et al. (US 2003/0155642).

Crafts discloses a method of designing an integrated circuit (IC), said method comprising: creating a representation of a shielding mesh in at least one layer (top layer 12) of said IC, said shielding mesh having a first plurality of lines (stippled shading in Fig. 5) which are designed to provide a first reference voltage V_{dd} and having a second plurality of lines (solid shading in Fig. 4) which are designed to provide a second reference voltage V_{ss}; and creating a representation of a plurality of signal lines

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(unshaded 53, 56; Fig. 6) routed through said shielding mesh, wherein at least one of said signal lines is coupled to a signal line on another layer (bottom layer 9 of Fig. 4) through one via (see signal path 3 of Fig. 7). Crafts does not disclose the at least one signal line coupled to a signal line on another layer through at least two vias. Davis et al. as described above discloses mesh-like interconnection structure comprising conductive lines (wirings) at different levels connected to each other by a plurality of conductive vias 47. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the structure of Crafts to have the at least one signal line coupled to a signal line on another layer through at least two conductive vias as taught by Davis et al. to provide both vertical and horizontal reinforcement that inhibit delamination of the layers and cracking.

Regarding claims 54 and 55, Crafts in view of Davis et al. does not specifically disclose the method performed by an electronic design automation (EDA) tool that uses code written in an HDL. However, EDA tool that uses code written in an HDL is a well-known method in the art to design integrated circuits. Therefore, designing the integrated circuit of Crafts in view of Davis et al. using known EDA tool employing code written in an HDL would have been obvious modification.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F. Tran whose telephone number is (571) 272-1665. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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January 6, 2006


THIENTRAN
PRIMARY EXAMINER